The Influence of Interface and Semiconductor Bulk Traps Generated Under HEFS on MOSFET`s Electrical Characteristics

Sanja Aleksić, Danijela Pantić, and Dragan Pantić

Abstract - In this paper, the impact of defects (donor and acceptor traps) which are generated at the Si/SiO_2 interface and in semiconductor bulk, when the gate oxide is exposed to a high electric field stress (HEFS), on n-channel MOS and VDMOS transistors electrical characteristics is analysed and simulated. Taking the advantage of simulation, it was shown how and why the generated traps affect on n-channel MOS and n-channel VDMOS electrical characteristics.[1]

Keywords – TCAD, traps, HEFS, interface, bulk, MOS.

I. Introduction

The stability and reliability of MOSFET`s electrical characteristics is one of the most important requirements that are requested in the process of device and circuit design. It is known that under the influence of different effects, such as irradiation, high temperature (NBTI) or high electric field stress (HEFS), the neutral or charged defects (traps) are generated at the Si/SiO_2 interface, as well as in the semiconductor and gate oxide bulk [1-3]. The formed traps may cause the temporal degradation of the electrical characteristics of semiconductor device, which finally affects on the reliable operation of the electronic circuit and device, where the MOSFETs are integrated.

Over the last few decades a number of the physical models for the instability explanations have been proposed [4,5]. The majority of these models have no ability to analyse influence of the all generated traps, considering that these very complex processes are still not well understood, since it is necessary to take into account the impact of a large number of parameters. Using the possibilities provided by Silvaco TCAD simulation tools, in which the advanced physical models are incorporated [6,7], the ability to separate analyse the influence of different parameters, models and mechanisms, on the device electrical characteristics is offered. The effects of interface and semiconductor bulk traps generated under the HEFS on the electrical characteristics of n-channel MOS and VDMOS transistors are investigated in this paper.

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II. Numerical Model

The presence of charged defects or traps at the Si/SiO_2 interface, or in oxide and semiconductor bulk has a significant impact on the device electrical characteristics. These traps are changing the density of space charge and the potential distribution in the device structure and also have the influence on the recombination statistics and carriers mobility. The fact is that the amount of bulk and interface charged traps increases significantly when the devices are exposed to high electric field or radiation (HEFS), and in these cases an accurate simulation of the electrical characteristics of semiconductor devices requires to take into consideration the influence of space charge that comes from stress induced charge traps.

There are three different mechanisms which add space charge directly into the right hand side of Poisson's equation in addition to the ionized donor and acceptor impurities, and these are interface fixed charge, interface trap and bulk trap states. Interface fixed charge is controlled by the interface boundary condition, while the interface and bulk charged traps, Q_{IT} and Q_{IB} are added directly into the Poisson`s equation:

$$div(\varepsilon\nabla\varphi) = q(n - p - N_D^+ + N_A^-) - (Q_{IT} + Q_{BT}) \quad (1)$$

Associated energy of interface and semiconductor traps lies in forbidden gap and exchange charge through the emission or captured electrons with conduction and valence band. The net charge Q_{IT} that comes from the presence on ionized donor-like (N_{DT}^+) and acceptor-like (N_{AT}^-) traps at Si/SiO2 interface is defined as:

$$Q_{IT} = q(N_{DT}^+ - N_{AT}^-) = Q_{DT}^+ - Q_{AT}^- \quad (2)$$

In the case when the associated energy of donor-like trap (DT) lies in forbidden gap near the bottom of conduction band it releases an electron and becomes positive charged. The increase of positive charge ($+Q_{IT}$) at the Si/SiO_2 interface reduces the threshold voltage V_{TH} of n-channel MOSFET (Fig. 1). Contrary, acceptor-like trap (AT) is ionized (negatively charged) when its energy level lies near the top of valence band. In that case, AT is filled with an electron, and the presence of $-Q_{IT}$ at the interface would cause an increase in the threshold voltage of n-channel MOSFET (Fig. 1). The changes of charge at the Si/SiO_2 interface also affects on other electrical characteristics such as: leakage current I_L, saturation current I_{SAT}, etc.

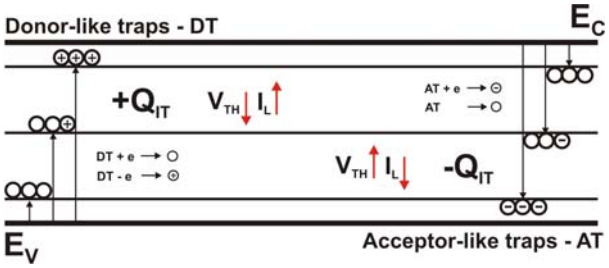

Fig. 1. The schematic representation of DT and AT ionization processes and the generation of the charge at Si/SiO_2 interface.

Traps generated under the HEFS in the semiconductor bulk influence on the electrical characteristics of MOSFET in a slightly different way. DT and AT ionization processes in the bulk of semiconductor are going on in a similar way and under the same conditions, but in this case the influence of electron concentration in the semiconductor bulk is more important than the formed positive or negative charge (Fig. 2). When the associated energy of DT in forbidden gap changes from E_V to E_C, the probability of its ionization increases, it releases an electron and becomes positive charged. The increase of the electron concentration in semiconductor bulk leads to the reduction of threshold voltage V_{TH}, while at the same time the saturation current I_{SAT} of the n-channel MOSFET increases. In the case of AT, the ionization probability increases when their associated energy changes from E_C to E_V. AT in semiconductor bulk captures an electron and becomes neutral. This recombination process significantly reduces the saturation current I_{SAT}, which is particularly important in n-channel VDMOSFET, due to the fact that its current after the channel, flows vertically through the epitaxial layer and Si substrate to drain contact.

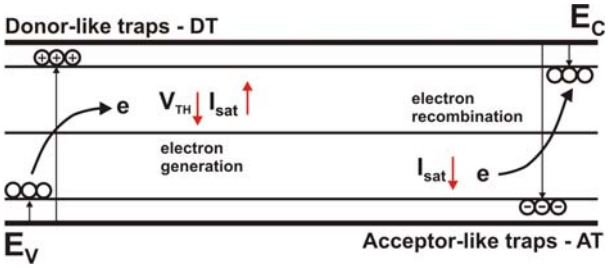

Fig. 2. The schematic representation of DT and AT ionization and generation-recombination processes in semiconductor bulk.

III. Simulation Results

In this section the impacts of DT and AT traps at Si/SiO_2 interface and in semiconductor bulk on the electrical characteristics of n-channel MOS transistor and n-channel VDMOS power transistor are presented. The simulations have been carried out by using the process simulator ATHENA [8] and the device simulator ATLAS [9], which are the integral part of Silvaco TCAD software package.

A. n-channel MOS transistor – interface traps

The impact of DT and AT generated at the Si/SiO_2 interface generated under HEFS is analysed on typical n-channel MOS transistor fabricated in standard 0.35μm CMOS technology. The gate oxide thickness is d_{OX}=10nm. The influences of interface DT and AT on V_{TH}, $I_L=I_D(V_{GS}=0.1V)$ and $I_{SAT}=I_D(V_{GS}=5.V)$, obtained by analysing the simulation results are summarized in Tab. I.

TABLE I: The influence of interface DT and AT on the electrical characteristics of n-channel MOS transistor.

	V_{TH}	I_L	I_{SAT}
$N_{DT} > 10^{14}cm^{-3}$ ↑	↓	↑	const
$E.L_{DT} > 0.6eV \rightarrow E_C$	↓	↑	const
$E.L_{DT} > 0.6eV \rightarrow E_V$	const	const	const
$N_{AT} > 10^{11}cm^{-3}$ ↑	↑	↓	↓
$E.L_{AT} > 0.8eV \rightarrow E_C$	↓	const	const
$E.L_{AT} > 0.8eV \rightarrow E_V$	const	↓	const

The distribution of potential in poly-Si, electric field in gate oxide, ionized DT density at Si/SiO_2 interface, and electron concentration in silicon, are shown on Fig. 3. The change of the threshold voltage V_{TH} of n-channel MOS, depending on interface DT parameters (donor trap density N_{DT} and associated energy level $E.L_{DT}$) is given on Fig. 4.

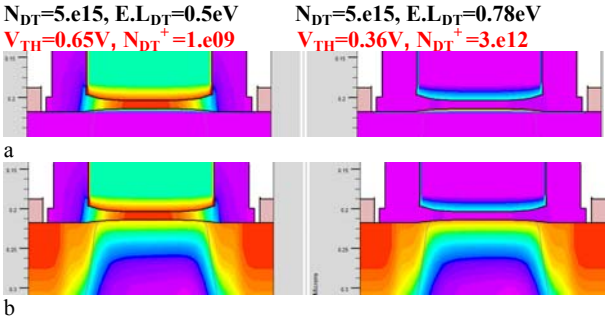

Fig. 3. Interface DT influence on n-channel MOS transistor: a) ionized donor traps density, b) electron concentration.

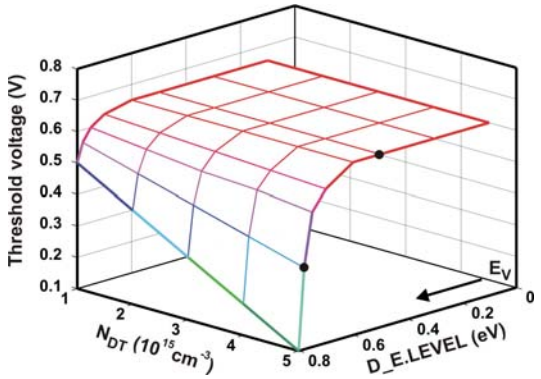

Fig. 4. The change of the threshold voltage V_{TH} of n-channel MOS, depending on interface DT parameters.

The distribution of potential in poly-Si, electric field in gate oxide, ionized AT density at Si/SiO_2 interface and electron concentration in silicon, are shown on Fig. 5. The changes of the threshold voltage V_{TH} and leakage current I_L of n-channel MOS, depending on interface AT parameters (acceptor trap density N_{AT} and associated energy level $E.L_{AT}$) are given on Fig. 6 and Fig. 7, respectively. Sets of AT parameters for the given ionized acceptor trap density and electron concentration on Fig. 5 are marked on Fig. 6.

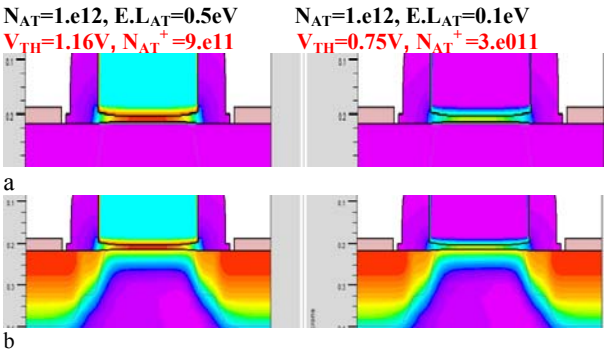

Fig. 5. Interface AT influence on n-channel MOS transistor: a) ionized acceptor traps density, b) electron concentration.

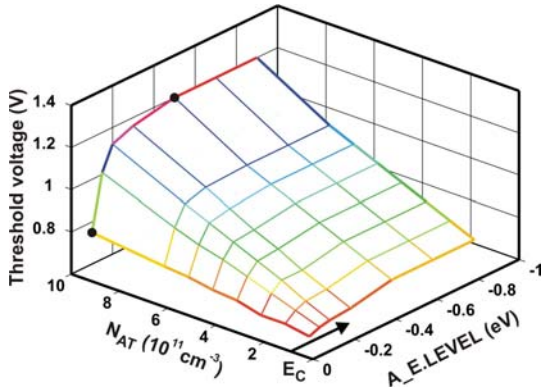

Fig. 6. The change of the threshold voltage V_{TH} of n-channel MOS, depending on interface AT parameters.

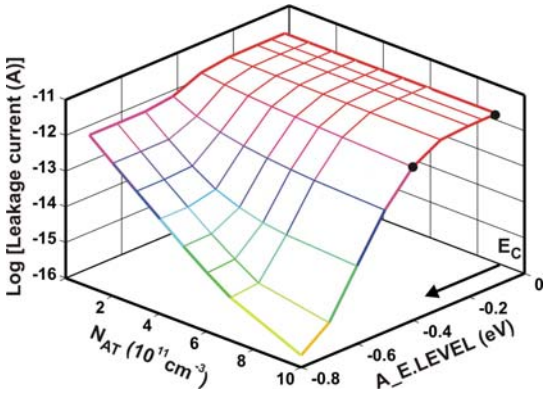

Fig. 7. The change of the leakage current I_L of n-channel MOS, depending on interface AT parameters.

B. n-channel MOS transistor – bulk traps

The influences of bulk DT and AT on V_{TH}, I_L and I_{SAT}, obtained by the analysing of the simulation results are summarized in Tab. II. It is obvious that the presence of DT and AT in semiconductor bulk also impact on the value of I_{SAT} due to recombination process.

TABLE II: The influence of bulk DT and AT on the electrical characteristics of n-channel MOS transistor.

	V_{TH}	I_L	I_{SAT}
$N_{DT} > 10^{16}cm^{-3}$ ↑	↓	↑	↑
$E.L_{DT} > E_V \rightarrow E_C$	↓	↑	↑
$N_{AT} > 10^{16}cm^{-3}$ ↑	↑	↓	↓
$E.L_{AT} > E_C \rightarrow E_V$	↑	↓	↓

The distribution of potential in poly-Si, electric field in gate oxide, ionized DT density in semiconductor bulk, electron concentration and total current density, in silicon are given on Fig. 8, while the change of the threshold voltage V_{TH} of n-channel MOS, depending on bulk DT parameters (donor trap density N_{DT} and associated energy level $E.L_{DT}$) is given on Fig. 9. Sets of DT parameters for the given ionized donor trap density, electron concentration and total current density on Fig. 8 are marked on Fig. 9.

The distribution of potential in poly-Si, electric field in gate oxide, ionized AT density in semiconductor bulk, electron concentration and carrier recombination velocity in silicon, are shown on Fig. 10, while the change of the threshold voltage V_{TH} of n-channel MOS, depending on bulk AT parameters (donor trap density N_{DT} and associated energy level $E.L_{DT}$) is given on Fig. 11.

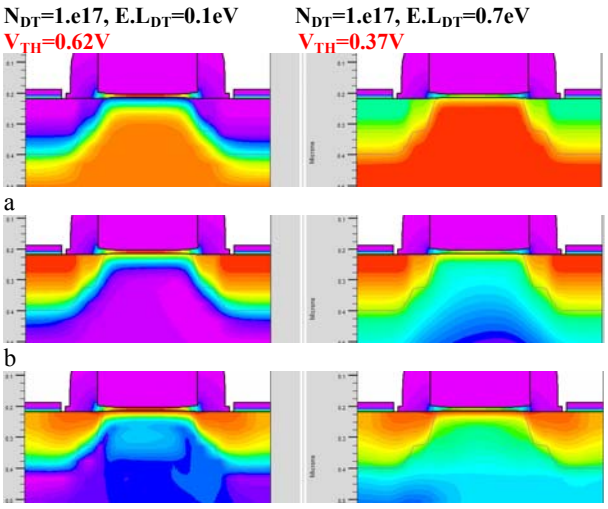

Fig. 8. Bulk DT influence on n-channel MOS transistor: a) ionized donor traps density, b) electron concentration and c) total current density.

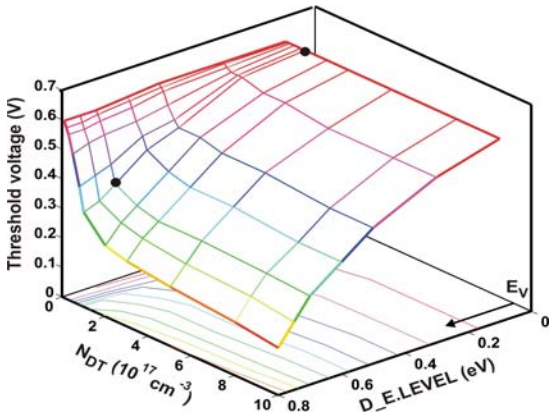

Fig. 9. The change of the threshold voltage V_{TH} of n-channel MOS, depending on bulk DT parameters.

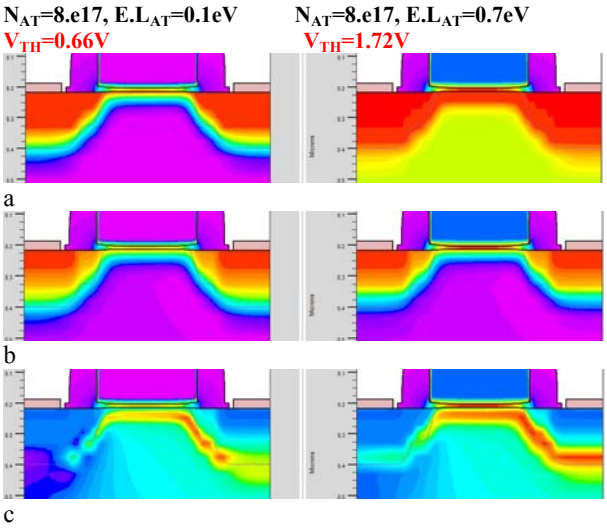

Fig. 10. Bulk AT influence on n-channel MOS transistor: a) ionized acceptor traps density, b) electron concentration and c) recombination velocity.

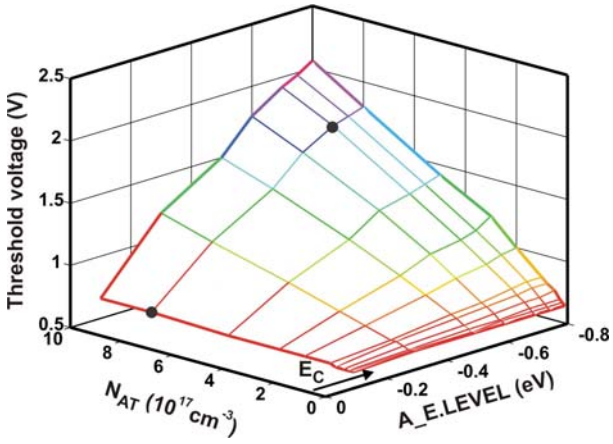

Fig. 11. The change of the threshold voltage V_{TH} of n-channel MOS, depending on bulk AT parameters.

C. n-channel VDMOS transistor – interface traps

The impact of DT and AT generated at the Si/SiO_2 interface generated under HEFS is analysed on typical n-channel VDMOS transistor. The channel length and gate oxide thickness of the VDMOS transistor are l_{CH}=1μm and d_{OX}=60nm, while the threshold voltage is V_{TH}=3.7V. The influences of interface DT and AT on V_{TH}, $I_L=I_D(V_{GS}=0.4V)$ and $I_{SAT}=I_D(V_{GS}=10.V)$, obtained by analysis of the simulation results are given in Tab. III.

TABLE III: The influence of interface DT and AT on the electrical characteristics of n-channel VDMOS transistor.

	V_{TH}	I_L	I_{SAT}
$N_{DT} >$ $10^{12}cm^{-3}$ ↑	↓	↑	const
$E.L_{DT} > 0.6eV \rightarrow E_C$	↓	↑	const
$E.L_{DT} > 0.6eV \rightarrow E_V$	const	↓	const
$N_{AT} >$ $10^{11}cm^{-3}$ ↑	↑	const	↓
$E.L_{AT} > 0.8eV \rightarrow E_C$	↓	const	↓
$E.L_{AT} > E_V \rightarrow 0.8eV$	const	const	↓

As can be seen, the interface DT has the identical impact on the electrical characteristics of VDMOS transistor as in the case of MOS transistor, while the impact of interface AT is slightly different. Unlike MOS transistor, here, the interface AT reduces the saturation current and does not affect on the leakage current.

The distribution of potential in poly-Si, electric field in gate oxide, ionized DT density at Si/SiO_2 interface, and electron concentration, are shown on Fig. 12, while the change of the threshold voltage V_{TH} of n-channel VDMOS, depending on interface DT parameters (donor trap density N_{DT} and associated energy level $E.L_{DT}$) is given on Fig. 13. The values of threshold voltage V_{TH} and ionized interface DT concentration N_{DT}^+ are given on Fig.12, while the sets of DT parameters for the given ionized donor trap density and electron concentration on Fig.12 are marked on Fig.13.

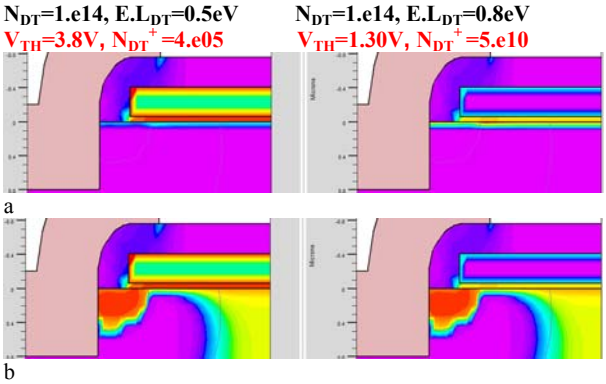

Fig. 12. Interface DT influence on n-channel VDMOS transistor: a) ionized donor traps density, b) electron concentration.

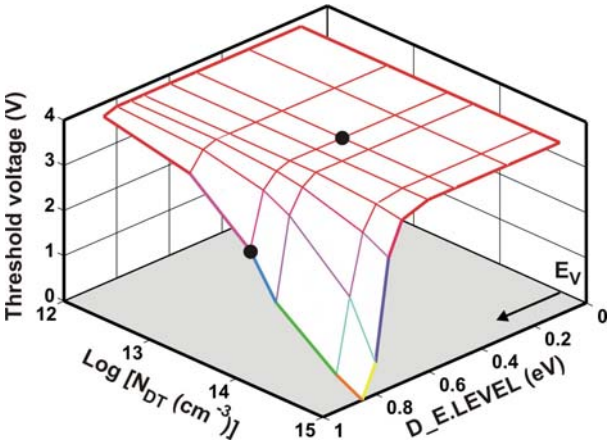

Fig. 13. The influence of interface DT parameters: donor trap density N_{DT} and energy level $E.L_{DT}$ on threshold voltage V_{TH}.

The distribution of potential in poly-Si, electric field in gate oxide, ionized AT density at Si/SiO_2 interface, and total current density, are shown on Fig. 14, while the change of the threshold voltage V_{TH} of n-channel VDMOS, depending on interface DT parameters (donor trap density N_{DT} and associated energy level $E.L_{DT}$) is given on Fig. 15.

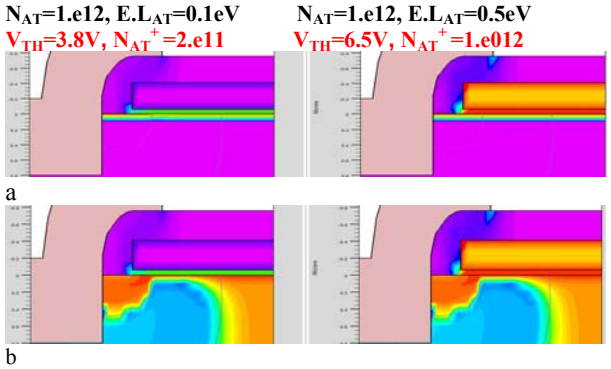

Fig. 14. Interface AT influence on n-channel VDMOS transistor: a) ionized acceptor traps density, b) total current density.

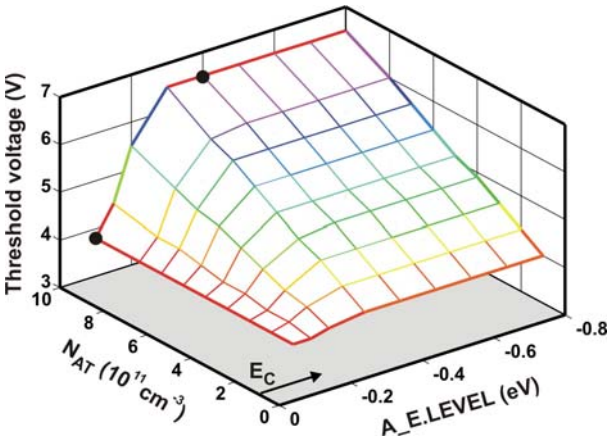

Fig. 15. The influence of interface AT parameters: acceptor trap density N_{AT} and energy level $E.L_{AT}$ on threshold voltage V_{TH}.

D. n-channel VDMOS transistor – bulk traps

The influences of bulk DT and AT on V_{TH}, I_L and I_{SAT}, obtained by the analysing of the simulation results are summarized in Tab. IV.

TABLE IV: The influence of bulk DT and AT on the electrical characteristics of n-channel VDMOS transistor.

	V_{TH}	I_L	I_{SAT}
N_{DT} > $10^{15}cm^{-3}$ ↑	↓	↑	↑
$E.L_{DT}$ > $E_V \rightarrow E_C$	↓	↓	↑
N_{AT} > $10^{??}cm^{-3}$ ↑	no inf.	↑	↓
$E.L_{AT}$ > $E_C \rightarrow$ 0.5eV	no inf.	const	↓
$E.L_{AT}$ > 0.5eV → E_V	no inf.	const	↓↓↓

The bulk DT has the identical impact on the electrical characteristics of VDMOS transistor as in the case of MOS transistor. The bulk AT reduces the saturation current due to ionization of traps and recombination of electrons. This is particularly evident when the associated energy of AT is approaching to the top of the valence zone (Fig. 16).

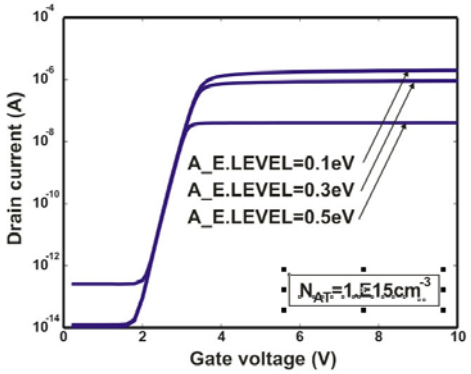

Fig. 16. The influence of bulk AT associate energy level on the saturation current of n-channel VDMOS transistor.

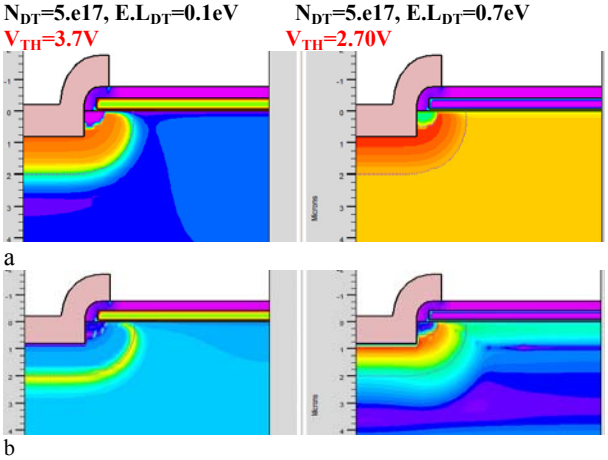

Fig. 17. Bulk DT influence on n-channel VDMOS transistor: a) ionized donor traps density, b) recombination velocity.

The distribution of potential in poly-Si, electric field in gate oxide, ionized DT and AT density in semiconductor bulk, electron concentration, recombination velocity and total current density, in silicon are given on Figs. 17 and 18, while the change of the threshold voltage V_{TH} of n-channel VDMOS, depending on bulk DT parameters is given on Fig. 19, where the sets of DT parameters for the given distributions are marked.

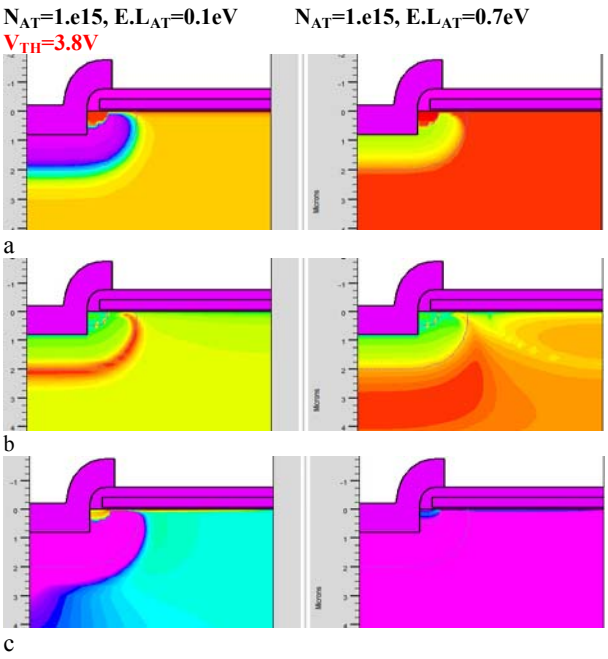

Fig. 18. Interface AT influence on n-channel VDMOS transistor: a) ionized acceptor traps density, b) recombination velocity, c) total current density.

IV. Conclusion

The impacts of defects, which are generated at the Si/SiO_2 interface and in the semiconductor bulk under HEFS, on the electrical characteristics of n-channel MOS and n-channel VDMOS power transistors are analysed and simulated separately by using the program ATHENA for the complete technology process simulation and the device simulator ATLAS which are an integral part of Silvaco TCAD software package.

Acknowledgement

This work has been supported by the Ministry of Education and Science of the Republic of Serbia, under the project TR 33035.

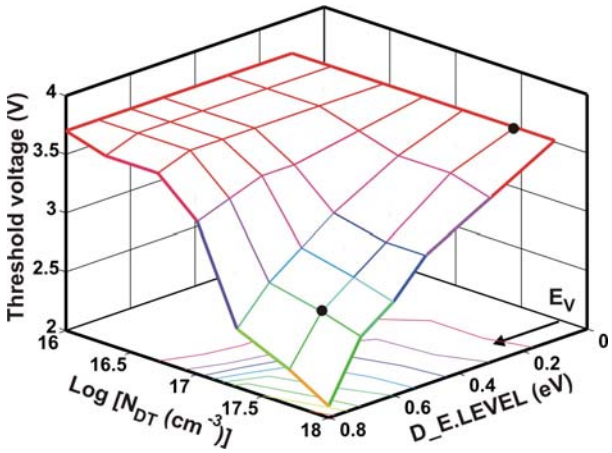

Fig. 19. The influence of interface DT parameters: donor trap density N_{DT} and energy level $E.L_{DT}$ on threshold voltage V_{TH}.

References

[1] Wang, T., Chiang, L., Zous, N., Chang, T., Huang, C., *"Oxide Traps in MOSFET's by Using a Subthreshold Transient Current Technique"*, IEEE Transaction on Electron Devices, Vol. 45, No. 8, 1998, pp. 1791-1796.

[2] Alwan, M., Beydoun, B., Ketata, K., Zoaeter, M., *"Bias temperature instability from gate charge characteristics investigations in n-channel power MOSFET"*, Microelectronics Journal, Vol. 38, 2007, pp. 727-734.

[3] Benlatreche, M.S,, Rahmoune, F., Toumiat, O., *"Experimental investigation of Si-SiO2 interface traps using equilibrium voltage step technique"*, Informacije MIDEM, Vol. 41, No. 3, 2011, pp. 168-170.

[4] Esseni, D., Bude, J-D., Selmi, L., *"On Interface and Oxide Degradation in VLSI MOSFETs—Part II: Fowler–Nordheim Stress Regime"*, IEEE Transaction on Electron Devices, Vol. 49, No. 2, 2002, pp. 254-263.

[5] Cartier, E., *"Characterization of the hot-electron-induced degradation in thin SiO_2 gate oxide"*, Microelectronics Reliability, Vol. 38, No. 2, 1997, pp. 201-211.

[6] Aleksić, S., Pešić, B., Pantić, D., *"Simulation of Semiconductor Bulk Trap Influence on the Electrical Characteristics of the n-channel Power VDMOS Transistor"*, Informacije MIDEM, Vol. 43, No. 2, 2013, pp. 124-130.

[7] Aleksić, S., Bjelopavlić, D., Pantić, D., *"Simulation of Bulk Traps Influence on the Electrical Characteristics of VDMOS Transistor*", Proc. of XLVI International Scientific Conference on Information, Communication and Energy Systems and Technologies - ICEST 2011, pp. 271-274, Niš, Serbia, June 2011.

[8] *ATHENA User's Manual*, SILVACO, Inc., CA, USA, 2013.

[9] *ATLAS User's Manual*, SILVACO, Inc., CA, USA, 2013.